

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board

Paper No. 34

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte KAZUYASU FUJISHIMA,  
YOSHIO MATSUDA and  
MIKIO ASAKURA

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Appeal No. 1999-0528  
Application 08/472,770

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HEARD: January 24, 2001

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Before THOMAS, HAIRSTON and LEVY, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellants have appealed to the Board from the examiner's final rejection of claims 19, 21, 22 and 23, which constitute all the claims remaining in the application.

Representative claim 19 is reproduced below:

19. A semiconductor memory device comprising:

a main memory divided into a plurality of blocks in the unit of a plurality of columns, including

a plurality of memory cells for storing information, arranged in a plurality of rows and a plurality of columns, each being formed of one transistor element and one capacitor element,

a plurality of word lines disposed in a plurality of rows, each having a plurality of memory cells arranged in a corresponding row connected thereto, and

a plurality of parallel-disposed bit line pairs, arranged in a plurality of columns, each having a plurality of memory cells arranged in a corresponding column connected thereto, and

a plurality of sense amplifiers arranged in a plurality of columns, and connected to a bit line pair of a corresponding column, for sensing and amplifying the potential difference appearing on said bit line pair of said corresponding column,

a data output line for providing data,

a plurality of circuits, each being provided corresponding to each block of said main memory, for providing or not providing information read out from a corresponding block of said main memory to said data output line, said plurality of circuits including a cache memory for storing the information read out from said main memory, said cache memory being arranged in a plurality of rows corresponding to said plurality of bit line pairs, and

a wiring arranged in a region adjacent said plurality of circuits, and connected to the circuits of said plurality of circuits,

wherein each block of said cache memory includes a plurality of storage elements arranged in a plurality of columns identical in number to said plurality of columns in each block of said main memory, for storing in block units information read out in block units from said main memory, said plurality of storage elements are aligned with said plurality of bit line pairs.

The following references are relied on by the examiner:

Matick et al. (Matick)	4,577,293	Mar. 18, 1986
Konishi et al. (Konishi)	4,809,230	Feb. 28, 1989 (filing date Dec. 4, 1986)
Ward et al. (Ward)	4,894,770	Jan. 16, 1990 (filing date June 1, 1987)

Claims 19, 21, and 22 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Matick. These same claims also stand rejected under 35 U.S.C. § 103 as being obvious over Ward alone. Finally, claim 23 stands rejected under 35 U.S.C. § 103 as being obvious over Matick or Ward, further in view of Konishi.

Rather than repeat the positions of the appellants and the examiner, reference is made to the brief and reply brief for appellants' positions, and the final rejection and answer for the examiner's positions.

OPINION

Generally for the reasons set forth by the examiner in the final rejection and answer, we sustain each of the rejections of all claims on appeal, further in view of the following embellishments of the examiner's views expressed in the answer. Appellants have submitted arguments only with respect to independent claim 19 in the context of the rejection under 35 U.S.C. § 102 over Matick and the rejection under 35 U.S.C. § 103 in view of Ward alone. No separate arguments have been presented as to either of these rejections for dependent claim 21 and independent claim 22. Additionally, appellants present no arguments as to dependent claim 23 at page 15 of the principal brief on appeal and rely for patentability upon the arguments presented for its respective parent claim 22. Thus, the rejection of claim 23 is also sustained.

For their part, the reply brief substantially duplicates the arguments presented in appellants' principal brief on appeal. We observe further that the responsive arguments portion of the answer directly addresses the three primary arguments of the appellants regarding the rejection under 35 U.S.C. § 102 over Matick and the single argument presented as to the rejection under 35 U.S.C. § 103 over Ward. We understand the examiner's reasoning in the answer as essentially responding to the rejection under 35 U.S.C. § 103 involving Ward in the same manner as he responded to the arguments presented with respect to the 35 U.S.C. § 102 rejection involving Matick.

As to the rejection involving Matick under 35 U.S.C. § 102, it appears that appellants' principal argument is that this reference does not expressly describe bit lines of the storage array or the arrangement of the latches in the row buffer 15. Appellants disagree with the examiner's view that each latch in the buffer memory 15 must be aligned with the bit line pairs in the same manner in order to receive the data from the bit lines from the DRAM storage array. We are unpersuaded of appellants' arguments.

The abstract of Matick indicates twice that the disclosed invention has a large bandwidth between the main memory and the cache memory stated to be "the usual on-chip interconnecting lines which avoids pin input/output problems." This bandwidth architecture is described in detail beginning at column 4, line 15. The background of the invention portion at column 1 of Matick indicates that a deficiency of the prior art on-chip cache memories of the prior art at that time was that they had a very limited bandwidth capability, which is essentially a limited bus width between the main memory and the cache memory.

The showing in figure 1 of Matick indicates to us that the latches described in the specification to comprise the master register and slave registers respectively both comprising the buffer 15 to be directly interconnected respectively to each bit decoder for each bit line of the storage array comprising the DRAM above the cache memory in this

figure. Note the depiction in the figure with respect to the individual interconnect-ability of the lines from the bit decoder through the isolators to the master register 22. In this light, note also the teachings at column 3, lines 30 through line 35. Within these lines there is stated the “master/slave row buffer 15 comprises a master register 22 and a slave register 23 each N bits wide corresponding to the width of the storage array and each composed of master/slave latches.” (Emphasis added). As indicated earlier at lines 30 through 31 and at column 4, lines 3 and 4 the master register receives an entire row of data from the storage array comprising the DRAM above it in figure 1. Thus, we conclude that the latches comprising the master register 22 and slave register 23 correspond to the claimed storage elements of representative claim 19 on appeal and are aligned directly with respect to the respective bit/column lines of the DRAM array above it as the examiner asserts and is claimed.

The teachings in Matick make clear that the bandwidth is so wide, that is, the bussing between the master and slave registers in the DRAM array itself is so wide, that there is no interconnectability problem between them. Thus, the discussion at the middle of page 11 of the brief pertains only to the architecture with respect to the relationship of the master and slave registers but not between the DRAM array itself and the cache as a whole as represented by buffer 15. The argument by appellants that the artisan would not appreciate the pitch of the bit lines being representative in this reference in the detail

required by the claim is based on speculation and traversed by the noted teachings above that we have outlined from the reference itself.

We are unpersuaded of appellants' second argument at page 12 of the brief that the slave register 23 and the master register 22 comprise a single buffer. Appellants' urging the Matick's real buffer does not comprise an arrangement of a plurality of rows is misplaced because the single buffer comprises two separate registers which can be clearly considered to be separate row registers that receive data dumped successively by row from the DRAM storage array into the master register first and from the master register into the slave register. In any event, the examiner has asserted and appellants have noted at page 9 of the brief that column 7, lines 49 through 53 of Matick indicate that there maybe "more than one row buffer per chip."

Additionally, we note that figure 2 shows that the cache memory comprising the buffer 15, which in turn comprises the master and slave registers 22 and 23, has the capacity of 512 bits which is double the arrangement of a single row of the 256 K bit DRAM array itself. Thus, each of the respective master and slave registers comprise 256 bits or one row of the DRAM array itself. This also argues for a proper consideration of the reference indicating an alignment of the storage positions in the master and slave registers comprising the cache with those particular positions correspondingly located in the DRAM array itself.

Finally, in response to appellants' third argument that Matick's memory array is not divided into a plurality of blocks as claim 19 requires, the examiner has asserted that it does and indicates at page 5 of the answer that the claimed "blocks" correspond to plural banks 1 through 4 shown in figure 2 or all of the 32 chips comprising a single bank represented in this figure. It is also indicated at column 4, lines 47 through 49 of Matick that "[t]he slaves on the various banks will normally be loaded with the desired working set blocks being accessed by the CPU." Therefore, in view of the foregoing arguments embellishing those positions set forth by the examiner in the final rejection and answer, we sustain the rejection of representative claim 19 as being anticipated by Matick under 35 U.S.C. § 102.

We turn next to the rejection of claims 19, 21 and 22 under 35 U.S.C. § 103 as being obvious over Ward. In considering the teachings and showings of Ward from our study of it, we disagree with appellants' arguments presented as to this rejection at pages 13 through 15 of the principal brief on appeal. We agree with appellants' assessment that Ward appears to show but does not appear to discuss that the DRAM array comprising the main memory of figure 1 of this reference is divided into plural or four columns or blocks where there are plural chips 14 comprising the entire bank 12.

We disagree with appellants' assertion that the artisan would recognize that each row buffer 16 has a size corresponding to the size of the single DRAM block and therefore

does not in effect store an entire row of the DRAM array itself. The abstract clearly states that “[e]ach static data buffer is connected to the memory array to receive and store a row of data from any addressed row of the array.” Even in accordance with the prior art discussed at column 1, lines 24 through 27, Ward states that “[a]n entire row of the two-dimensional array, dictated [sic] by high-order address bits, is loaded into the row buffer on the row address strobe (RAS) signal.” Note also the teachings at column 2, lines 15 through 24. Finally, we note column 3, lines 50 through 54 state that an “advantage of the system over conventional cache systems is that a full row of data from adjacent storage elements, not just a single bit per memory chip, can be addressed and held in the buffers which serve as cache memory.”

Thus, we are in agreement with the examiner's view that the alignment taught to the artisan within 35 U.S.C. § 103 from this reference is the same alignment broadly recited in the claims on appeal. We observe that appellants' admitted prior art figure 1 has more details regarding the memory array itself as comprising word lines and bit line pairs. The noted teachings in Ward taken alone, or further in view of what is well-known in the art as represented by appellants' admitted prior art figure 1 for the details of the construction of the DRAM and memory array itself, would have indicated to the artisan the alignment of the type recited in the representative independent claim 19 on appeal.

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In view of the foregoing, the decision of the examiner rejecting claims 19, 21, 22, and 23 variously under 35 U.S.C. § 102 and 35 U.S.C. § 103 is affirmed.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

James D. Thomas	)	
Administrative Patent Judge	)	
	)	
	)	
	)	BOARD OF PATENT
Kenneth W. Hairston	)	
Administrative Patent Judge	)	APPEALS AND
	)	
	)	INTERFERENCES
	)	
Stuart S. Levy	)	
Administrative Patent Judge	)	

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